

CORRECTED VERSION

(19) World Intellectual Property  
Organization  
International Bureau



(43) International Publication Date  
26 February 2004 (26.02.2004)

PCT

(10) International Publication Number  
WO 2004/017512 A1

- (51) International Patent Classification<sup>7</sup>: H03F 1/02
- (21) International Application Number:  
PCT/IB2003/003278
- (22) International Filing Date: 18 July 2003 (18.07.2003)
- (25) Filing Language: English
- (26) Publication Language: English
- (30) Priority Data:  
02078421.1 19 August 2002 (19.08.2002) EP
- (71) Applicant (for all designated States except US): KONINKLIJKE PHILIPS ELECTRONICS N.V. [NL/NL]; Groenewoudseweg 1, NL-5621 BA Eindhoven (NL).
- (72) Inventor; and
- (75) Inventor/Applicant (for US only): BLEDNOV, Igor, I. [RU/NL]; c/o Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).
- (74) Agent: MAK, Theodorus, N.; Philips Intellectual Property & Standards, Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).

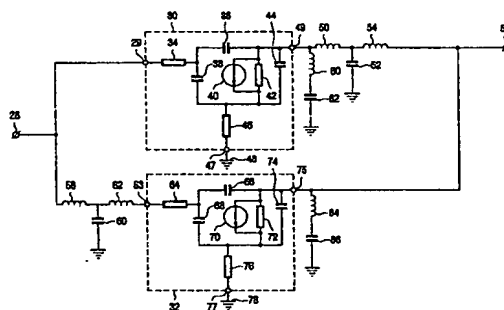
- (81) Designated States (national): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.
- (84) Designated States (regional): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declaration under Rule 4.17:

— as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii)) for the following designations AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PG, PH,

[Continued on next page]

(54) Title: HIGH POWER DOHERTY AMPLIFIER



(57) Abstract: A high power Doherty amplifier circuit having at least one input terminal and at least one output terminal comprising at least one carrier transistor (30) forming a main amplifier stage; at least one peak transistor (32) forming a peak amplifier stage; a first input line (27) connecting the input terminal (28) to an input (29) of the carrier transistor (30); a second input line (31) connecting the input terminal (28) to an input (63) of the peak transistor (32); a first output line (33) connecting the output terminal (56) to an output (49) of the carrier transistor (30); and a second output line (35) connecting the output terminal (56) to an output (75) of the peak transistor (32). A high power Doherty amplifier circuit package comprising a support structure (104) supporting circuit elements of the Doherty amplifier circuit; at least one input terminal (102) and at least one output terminal (96) both terminals being supported on the support structure (104); at least one carrier transistor (92) forming a main amplifier stage and at least one peak transistor (98) forming a peak amplifier stage both transistors being supported on the support structure (104); a first input network (106) connecting the input terminal (102) to an input of the carrier transistor (92); a second input network (100, 114, 116) connecting the input terminal (102) to an input of the peak transistor (98); a first output network (94, 108, 110) connecting the output terminal (96) to an output of the carrier transistor (92); and a second output network (112) connecting the output terminal (96) to an output of the peak transistor (98), and wherein the input and output networks are artificial transmission lines comprising serial circuits and / or parallel circuits of at least one capacitance and / or at least one inductance.